3. (Amended) A method for etching a semiconductor substrate using a germanium hard mask, the semiconductor substrate having at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of metallic germanium over the at least one dielectric layer;

b) patterning the layer of metallic germanium to form the germanium hard mask as a top most layer over the at least one dielectric layer, the patterning step comprising:

i) depositing a photo resist layer over the layer of metallic germanium;

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

iii) etching the layer of metallic germanium through the photolithography image; and

iv) removing the photo resist layer prior to selectively etching the at least one dielectric layer through the germanium hard mask;

c) selectively etching the at least one dielectric layer through the germanium hard mask with the germanium hard mask as a top most layer to form an opening in the at least one dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the at least one dielectric layer; and

e) removing the layer of metallic germanium after performing the step of selectively etching the at least one dielectric layer and before performing the step of selectively etching the semiconductor substrate.

4. (Amended) The method as claimed in claim 5, the step of removing the layer of germanium oxide including rinsing the semiconductor substrate in water.

5. (Amended) The method as claimed in claim 3, the step of removing the layer of metallic germanium including:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and

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removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

6. (Amended) The method as claimed in claim 3, wherein the step of oxidizing the layer of metallic germanium. includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

8. (Amended) The method as claimed in claim 3, further comprising the step of forming the at least one dielectric layer which includes the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

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depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

11. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

a) depositing a metallic germanium layer on a dielectric stack, the dielectric stack having a plurality of dielectric layers disposed on a semiconductor substrate;

b) patterning the metallic germanium layer to form a germanium hard mask as a top most layer over the dielectric stack, the patterning step comprising:

i) depositing a photo resist layer over the metallic germanium layer;

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image; and

iii) etching the metallic germanium layer through the photolithography image;

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c) removing the photo resist layer prior to etching the dielectric stack through the germanium hard mask;

d) etching the dielectric stack through the germanium hard mask with the germanium hard mask as a top most layer to form a dielectric hard mask over the major surface of the semiconductor substrate;

e) etching the semiconductor substrate through the dielectric hard mask;

f) forming doped regions in the semiconductor substrate; and

g) forming dielectric and conductive structures over the semiconductor substrate; and

h) removing the metallic germanium layer after the step of etching the dielectric stack and before the step of etching the semiconductor substrate, wherein the step of removing the metallic germanium layer includes the steps of:

oxidizing the metallic germanium layer, and

rinsing the semiconductor substrate in water after performing the step of oxidizing

the metallic germanium layer.

12. (Previously Amended) The method as claimed in claim 11, wherein the step of depositing a metallic germanium layer includes depositing the metallic germanium layer having a thickness between approximately 40 nm and approximately 500 nm in a chemical vapor deposition process.

E3 cont.

14. (Amended) The method as claimed in claim 11, further comprising the step of forming the dielectric stack including the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm on the major surface of the semiconductor substrate;

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depositing a nitride layer having a thickness between 50 nm and approximately 300 nm on the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3000 nm on the nitride layer.

19. (Amended) A method for etching a semiconductor wafer, comprising the steps of:

a) forming a germanium hard mask as a top most layer over the dielectric stack, the dielectric stack having a plurality of dielectric layers disposed on a major surface of the semiconductor wafer, the step of forming a germanium hard mask comprising:

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depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40nm over the dielectric stack,

depositing a photo resist layer over the layer of metallic germanium,

exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography mask, and

etching the layer of metallic germanium through the photolithography mask;

b) removing the photo resist layer prior to etching the dielectric stack through the germanium hard mask;

c) etching the dielectric stack through the germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor wafer; and

d) etching the semiconductor wafer through the dielectric hard mask; and

ES cont.

e) removing the germanium hard mask after etching the dielectric stack and before etching the semiconductor wafer, wherein the step of removing the germanium hard mask includes the steps of:

oxidizing the layer of metallic germanium to convert the layer of metallic germanium into a layer of germanium oxide, and

removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

20. (Previously Amended) The method as claimed in claim 19, wherein the step of removing the layer of germanium oxide includes rinsing the semiconductor wafer in water.

21. (Amended) The method as claimed in claim 19, wherein the step of oxidizing the layer of metallic germanium. includes heating the semiconductor substrate at elevated temperature in an

environment of ambient oxygen.

26. (Amended) A method for etching a semiconductor substrate having at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the at least one dielectric layer;

b) depositing a photo resist layer over the layer of germanium;

c) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

d) etching the layer of germanium through the photolithography image to form a germanium hard mask over the at least one dielectric layer;

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e) removing the photo resist layer from over the germanium hard mask;

f) patterning the at least one dielectric layer through the germanium hard a mask to form a dielectric hard mask over the semiconductor substrate; and

g) selectively etching the semiconductor substrate through the dielectric hard mask; and

h) removing the germanium hard mask, comprising the steps of: oxidizing the layer of germanium to form a layer of germanium oxide therefrom, and removing the layer of germanium oxide after performing the step of oxidizing the layer of metallic germanium.

27. The method as claimed in claim 26, wherein removing the layer of germanium oxide comprises rinsing the semiconductor substrate in water.

28. (Amended) The method as claimed in claim 26, wherein oxidizing the layer of germanium

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includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

E7 Cont

30. (Amended) The method as claimed in claim 26, further comprising forming the at least one dielectric layer by:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

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depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

32. (Amended) A method for etching a semiconductor substrate having at least one dielectric layer over a major surface thereof, the method comprising the steps of:

a) depositing a layer of germanium over the at least one dielectric layer;

b) patterning the layer of germanium to form a germanium hard mask, the step further comprising:

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i) depositing a photo resist layer over the layer of germanium;

ii) exposing the photo resist layer to light and developing the exposed photo resist layer to form a photolithography image;

iii) etching the layer of germanium through the photolithography image; and

iv) removing the photo resist layer prior to selectively etching the at least one

dielectric layer through the germanium hard mask;

c) patterning the at least one dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the at least one dielectric layer; and

d) selectively etching the semiconductor substrate through the opening in the at least one dielectric layer.

E9 cont.

33. (New) The method as claimed in claim 3, wherein oxidizing the layer of metallic germanium. includes oxidizing the layer of metallic germanium in an anodic oxidation process having a time duration, and wherein the anodic oxidation process comprises: heating the semiconductor wafer at an elevated temperature in an environment of ambient oxygen; and applying an electric bias to the layer of metallic germanium.

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34. (New) The method as claimed in claim 33, wherein the time duration depends on the thickness of the layer of metallic germanium, the applied electric bias, and the elevated temperature.

35. (New) The method as claimed in claim 3, wherein the at least one dielectric layer comprises a plurality of dielectric layers.

36. (New) The method as claimed in claim 11, wherein oxidizing the metallic germanium.layer includes heating the semiconductor substrate at elevated temperature in an environment of ambient oxygen.

37. (New) The method as claimed in claim 11, wherein oxidizing the metallic germanium.layer includes oxidizing the metallic germanium layer in an anodic oxidation process having a time duration, and wherein the anodic oxidation process comprises: heating the semiconductor substrate at an elevated temperature in an environment of ambient oxygen; and applying an electric bias to the metallic germanium layer.

38. (New) The method as claimed in claim 37, wherein the time duration depends on the thickness of the metallic germanium layer, the applied electric bias, and the elevated temperature.

E 10 cont.

39. (New) The method as claimed in claim 19, wherein oxidizing the layer of metallic germanium. includes oxidizing the layer of metallic germanium in an anodic oxidation process having a time duration, and wherein the anodic oxidation process comprises: heating the semiconductor wafer at an elevated temperature in an environment of ambient oxygen; and applying an electric bias to the layer of metallic germanium.

40. (New) The method as claimed in claim 26, wherein oxidizing the layer of germanium. includes oxidizing the layer of germanium in an anodic oxidation process having a time duration, and wherein the anodic oxidation process comprises: heating the semiconductor substrate at an elevated temperature in an environment of ambient oxygen; and applying an electric bias to the layer of germanium.

41. (New) The method as claimed in claim 40, wherein the time duration depends on the